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Atty. Docket No. MP0227
Application No: 10/619,278

Amendments to the Claims

Please cancel Claims 72, 77 and 80, add new Claims 84-86, and amend the remaining claims as follows:

1. (Currently Amended) A clock recovery adjustment circuit configured to adjust a clock signal recovered from a data stream, comprising:

a) a clock phase adjustment circuit, ~~receiving clock phase information and~~ providing a clock phase adjustment signal, said clock phase adjustment circuit comprising parallel first and second clock phase adjustment paths configured to receive said clock phase information, said first clock phase adjustment path comprising a first multiplier and providing a first clock phase adjustment path signal, and said second clock phase adjustment path comprising a second multiplier and a first integrator and providing a second clock phase adjustment path signal;

b) a clock frequency adjustment circuit, receiving clock frequency information and providing a clock frequency adjustment signal;

c) logic configured to (i) sample said data stream at predetermined times, (ii) receive a plurality of predetermined phases of said clock signal, and (iii) provide said clock frequency information and said clock phase information from sampled data and said predetermined phases of said clock signal; and

d) an adder circuit, receiving said clock phase adjustment signal and said clock frequency adjustment signal, and providing a clock recovery adjustment signal.

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2. (Currently Amended) The clock recovery adjustment circuit of Claim 11, wherein said clock frequency adjustment circuit comprises a ~~first~~ third multiplier and a ~~first~~ second integrator.

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3. (Currently Amended) The clock recovery adjustment circuit of Claim 2, wherein said ~~first~~ third multiplier receives said clock frequency information.

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4. (Currently Amended) The clock recovery adjustment circuit of Claim ~~3~~ 13, wherein said ~~first~~ third multiplier and said ~~first~~ second integrator are in series.

5. (Currently Amended) The clock recovery adjustment circuit of Claim ~~4~~ 14, wherein said ~~first~~ second integrator provides said clock frequency adjustment signal.

6. (Previously Presented) The clock recovery adjustment circuit of Claim 11, configured to adjust a clock signal recovered from a data stream.

7. (Previously Presented) The clock recovery adjustment circuit of Claim 1, wherein said clock frequency information comprises (i) an undershoot determination and (ii) an overshoot determination relative to a bit length of said data stream.

8. (Previously Presented) The clock recovery adjustment circuit of Claim 1, wherein said clock phase information comprises (i) an early clock phase determination and (ii) a late clock phase determination relative to a data transition of said data stream.

9. (Previously Presented) The clock recovery adjustment circuit of Claim 11, further comprising logic configured to (i) sample said data stream at predetermined times and (ii) provide said clock frequency information and said clock phase information from sampled data.

10. (Original) The clock recovery adjustment circuit of Claim ~~9~~ 17, wherein said logic is configured to receive a plurality of predetermined phases of said clock signal.

11. (Currently Amended) A clock recovery adjustment circuit, comprising:

a) a clock phase adjustment circuit, receiving clock phase information and providing a clock phase adjustment signal, comprising parallel first and second clock phase adjustment paths configured to receive said clock phase information, said first

clock phase adjustment path comprising a ~~second~~ first multiplier and providing a first clock phase adjustment path signal, and said second clock phase adjustment path comprising a ~~third~~ second multiplier and a ~~second~~ first integrator and providing a second clock phase adjustment path signal;

b) a clock frequency adjustment circuit, receiving clock frequency information and providing a clock frequency adjustment signal; and

c) an adder circuit, receiving said clock phase adjustment signal and said clock frequency adjustment signal, and providing a clock recovery adjustment signal.

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12. (Original) The clock recovery adjustment circuit of Claim 11, wherein said adder circuit comprises a first adder and a second adder.

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13. (Original) The clock recovery adjustment circuit of Claim ~~12~~, wherein said first adder is configured to (i) add said clock frequency adjustment signal and said second clock phase adjustment path signal, and (ii) provide a first adder output.

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14. (Original) The clock recovery adjustment circuit of Claim ~~13~~, wherein said second adder is configured to (i) add said first adder output and said first clock phase adjustment path signal, and (ii) provide said clock recovery adjustment signal.

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15. (Previously Presented) A clock data recovery circuit, comprising:

a) the clock recovery adjustment circuit of Claim 11;

b) a clock recovery circuit, configured to sample a data stream and provide (i) a recovered clock signal and (ii) said clock phase information and said clock frequency information from sampled data.

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16. (Original) The clock data recovery circuit of Claim ~~15~~, wherein said clock recovery circuit comprises a plurality of latches configured to sample said data stream at predetermined times.

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17. (Original) The clock data recovery circuit of Claim 16, wherein said predetermined times are at regular time intervals corresponding to an integer fraction of said recovered clock signal.

18. (Original) The clock data recovery circuit of Claim 17, wherein said integer fraction is $(1/2^n)$, where n is 0 or an integer of at least 1.

19. (Original) The clock data recovery circuit of Claim 16, wherein said clock recovery circuit further comprises a plurality of logic gates configured to generate said clock phase information and said clock frequency information from sampled data.

20. (Original) The clock data recovery circuit of Claim 15, further comprising a phase locked loop configured to generate a reference clock signal for locking said recovered clock signal.

21. (Currently Amended) A transceiver, comprising:

a) the clock data recovery circuit of Claim 11;

b) a transmitter communicatively coupled to said clock ~~data~~ recovery adjustment circuit, configured to transmit serial data to a network; and

c) a receiver communicatively coupled to said clock ~~data~~ recovery adjustment circuit, configured to receive serial data from said network.

22. (Original) The transceiver of Claim 21, embodied on a single integrated circuit.

23. (Original) The transceiver of Claim 21, further comprising a PLL configured to provide a reference clock signal to said transmitter and said receiver.

24. (Original) The transceiver of Claim 21, further comprising a function generator.

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25. (Original) The transceiver of Claim 24, wherein said function generator compriscs a spread spectrum wave generator.

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26. (Original) The transceiver of Claim 21, further comprising a configuration block configured to store and provide configuration information for said transceiver.

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27. (Previously Presented) A system for transferring data on or across a network, comprising:

a) the transceiver of Claim 21; 28

b) at least one transmitter port communicatively coupled to said transmitter for transmitting scrial data to an external receiver; and

c) at least one receivcr port communicatively coupled to said receiver for rceiving ~~said~~ a data stream.

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28. (Original) The system of Claim 27, wherein said data stream is a serial data stream.

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29. (Original) The system of Claim 28, further comprising a converter configured to convert said serial data stream into a parallel data stream.

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30. (Original) The system of Claim 29, further comprising a storage device configured to receive said parallel data stream.

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31. (Original) The system of Claim 27, wherein said system is part of a storage network.

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32. (Original) The system of Claim 27, configured to convert serial data from said network to parallel data for a storage device, and convert parallel data from said storage device to serial data for said nctwork.

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33. (Original) A network, comprising:

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a) a plurality of the systems of Claim 34, communicatively coupled to each other; and

b) a plurality of storage or communications devices, each of said storage or communications devices being communicatively coupled to one of said systems.

34. (Original) The network of Claim 40, wherein said at least one storage or communications device comprises a storage device.

35. (Previously Presented) A clock recovery adjustment circuit configured to adjust a clock signal recovered from a data stream, comprising:

a) means for adjusting a clock phase from clock phase information comprising parallel first and second clock phase adjustment paths configured to receive said clock phase information, said first clock phase adjustment path comprising a first means for multiplying, and said second clock phase adjustment path comprising a second means for multiplying and a first means for integrating;

b) means for adjusting a clock frequency from clock frequency information; and

c) means for providing a clock recovery adjustment signal, coupled to outputs of said means for adjusting said clock phase and said means for adjusting said clock frequency.

36. (Previously Presented) The clock recovery adjustment circuit of Claim 42, wherein said means for adjusting said clock frequency comprises a third means for multiplying and a second means for integrating in series.

37. (Cancelled)

38. (Previously Presented) The clock recovery adjustment circuit of Claim 42, wherein said clock frequency information comprises (i) an undershoot determination and (ii) an overshoot determination relative to a bit length of said data stream.

45 (Previously Presented) The clock recovery adjustment circuit of Claim 42, wherein said clock phase information comprises (i) an early clock phase determination and (ii) a late clock phase determination relative to a data transition of said data stream.

46 (Previously Presented) The clock recovery adjustment circuit of Claim 42, further comprising means for providing said clock frequency information.

47 (Original) The clock recovery adjustment circuit of Claim 46, further comprising means for sampling said data stream at predetermined times.

48 (Original) The clock recovery adjustment circuit of Claim 47, further comprising means for providing said clock phase information.

43. (Cancelled)

49 (Previously Presented) The clock recovery adjustment circuit of Claim 42, wherein said means for providing said clock recovery adjustment signal comprises first and second adders.

50 (Original) The clock recovery adjustment circuit of Claim 49, wherein said first and second adders are configured to add outputs of said means for adjusting said clock phase and said means for adjusting said clock frequency.

51 (Previously Presented) A clock data recovery circuit, comprising:

a) the clock recovery adjustment circuit of Claim 42; and

b) means for recovering a clock signal from a data stream, said clock signal having said clock phase and said clock frequency.

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47. (Original) The clock data recovery circuit of Claim 46, wherein said means for recovering comprises a means for sampling said data stream at predetermined times.

48. (Original) The clock data recovery circuit of Claim 47, wherein said means for sampling comprises a plurality of latches.

49. (Original) The clock data recovery circuit of Claim 47, wherein said means for recovering comprises means for generating said clock phase information and means for generating said clock frequency information from sampled data.

50. (Original) The clock data recovery circuit of Claim 47, further comprising a means for generating a reference clock signal.

51. (Original) A transceiver, comprising:

a) the clock data recovery circuit of Claim 47;

b) means for transmitting serial data to a network; and

c) means for receiving a serial data stream from said network.

52. (Original) The transceiver of Claim 51, further comprising means for providing a reference clock signal to said means for transmitting and said means for receiving.

53. (Original) The transceiver of Claim 51, embodied on a single integrated circuit.

54. (Original) A system for transferring data on or across a network, comprising:

a) the transceiver of Claim 51;

b) a first port communicatively coupled to said means for transmitting; and

c) a second port communicatively coupled to said means for receiving.

55. (Original) The system of Claim 54, further comprising a means for converting said serial data stream into parallel data.

56. (Original) The system of Claim 55, further comprising a means for storing said parallel data.

57. (Original) The system of Claim 55, wherein said system is part of a storage network.

58. (Original) The system of Claim 56, further comprising a means for converting said parallel data to serial data for said network.

59. (Original) A network, comprising:

a) a plurality of the systems of Claim 54, communicatively coupled to each other; and

b) a plurality of means for storing or further communicating data from said serial data stream, each of said means for storing or further communicating being communicatively coupled to one of said systems.

60. (Currently Amended) A method of adjusting a clock signal recovered from a data stream, comprising the steps of:

a) sampling said data stream at predetermined times;

b) generating clock frequency information and clock phase information from sampled data by logically comparing data sampled at two or more successive phases of a reference clock;

c) altering a frequency <u>of said clock signal in response to said clock frequency information</u> and~~/or~~ <u>altering</u> a phase of said clock signal in response to ~~said clock frequency information and~~ said clock phase information <u>received by parallel first and second clock phase adjustment paths, said first clock phase adjustment path comprising a first multiplier and providing a first clock phase adjustment path</u>

signal, and said second clock phase adjustment path comprising a second multiplier and a first integrator and providing a second clock phase adjustment path signal.

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61. (Original) The method of Claim 60, wherein said sampling comprises latching said data stream at predetermined intervals.

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62. (Original) The method of Claim 61, wherein said predetermined intervals are less than two data bit lengths.

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63. (Original) The method of Claim 62, wherein said predetermined intervals are about one data bit length or less.

64. (Canceled)

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65. (Original) The method of Claim 60, wherein said sampling is performed continuously.

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66. (Original) The method of Claim 60, wherein said sampling is performed periodically.

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67. (Original) The method of Claim 60, wherein said sampling is performed conditionally.

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68. (Currently Amended) The method of Claim 60, further comprising repeating said method until said clock signal is phase locked to a reference clock signal.

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69. (Currently Amended) The method of Claim 60, further comprising~~, after said altering step,~~ selecting a reference clock phase to provide to a phase detector receiving the data stream.

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70. (Original) The method of Claim 60, further comprising adjusting said clock frequency information by a frequency adjustment coefficient.

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71. (Currently Amended) The method of Claim 70, further comprising adjusting said clock phase information by a phase adjustment coefficient and/or a phase-frequency adjustment coefficient in at least one of the first and second clock phase adjustment paths.

72. (Canceled)

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73. (Currently Amended) A method of recovering a clock signal from a data stream, comprising the steps of:

a) receiving said data stream in a phase detector;

b) sampling said data stream at predetermined times;

c) generating clock frequency information and clock phase information from sampled data;

d) altering a frequency of said clock signal in response to said clock frequency information and/~~or~~ altering a phase of said clock signal in response to ~~said clock frequency information and~~ said clock phase information received by parallel first and second clock phase adjustment paths, said first clock phase adjustment path comprising a first multiplier and providing a first clock phase adjustment path signal, and said second clock phase adjustment path comprising a second multiplier and a first integrator and providing a second clock phase adjustment path signal; and

e) adjusting a frequency of a second clock signal in response to at least said clock frequency information.

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74. (Original) The method of Claim 73, further comprising providing said clock signal.

75. (Original) The method of Claim 73, further comprising providing said data stream from said phase detector.

76. (Currently Amended) The method of Claim 73, further comprising repeating said performing step until said clock signal is phase locked to a reference clock signal.

77. (Canceled)

78. (Previously Presented) The method of Claim 73, further comprising adjusting a phase of said second clock signal in response to at least said clock phase information.

79. (Currently Amended) The clock recovery adjustment circuit of Claim 1, wherein said clock frequency adjustment circuit comprises a ~~first~~ third multiplier and a ~~first~~ second integrator.

80. (Canceled)

81. (Previously Presented) The clock recovery adjustment circuit of Claim 1, wherein said adder circuit comprises a first adder and a second adder.

82. (Previously Presented) The clock recovery adjustment circuit of Claim 81, wherein said first adder is configured to (i) add said clock frequency adjustment signal and said second clock phase adjustment path signal, and (ii) provide a first adder output.

83. (Previously Presented) The clock recovery adjustment circuit of Claim 82, wherein said second adder is configured to (i) add said first adder output and said first clock phase adjustment path signal, and (ii) provide said clock recovery adjustment signal.

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84. (New) The clock data recovery adjustment circuit of Claim 1, wherein said logic comprises a plurality of latches configured to sample said data stream at regular time intervals corresponding to an integer fraction of said recovered clock signal.

85. (New) The clock data recovery adjustment circuit of Claim 84, wherein said integer fraction is $(1/2^n)$, where n is 0 or an integer of at least 1.

86. (New) A clock data recovery circuit, comprising the clock data recovery adjustment circuit of Claim 1, and a phase locked loop configured to generate a reference clock signal for locking said recovered clock signal.